REMARKS

Applicant has carefully reviewed the Office Action dated December 223, 2004. Claims 1-7 remain pending in this application. Applicant has amended Claims 1-7 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Claims 1-7 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Examiner has indicated that the language that refers to the "type" of memory access, these being a Read access, and Write access or an erase, is confusing. Applicant believes that the specification sets forth that there are two different memory accesses, a Read memory access and a Write/Erase memory access. Applicant refers to these two different memory access operations as "types" of operations in the claims. This is not an atypical way to refer to this in the industry. For example, in one of the cited references, U.S. Patent No. 6,681,300, at Col. 3, line 62, the memory is set forth as being optimized "based on a type of memory operation, i.e., a read or a write." It can be seen that even though the specification only refers to the Read and Write/Erase operations as being memory access operations, referring to them in the claim as being types of memory access operations is well understood in the industry. However, Applicant has removed the word "type" for clarification purposes, as Applicant believes that the claims set forth that there are at least two memory access operations that are selectable and definable by the lock bits. Therefore, Applicant believes that the claims as set forth are unambiguous with the presence or absence of the word "type." Therefore, Applicant respectfully requests the withdrawal of the 35 U.S.C. §112 rejection with respect to Claims 1-7.

Claim 7 has further been rejected under 35 U.S.C. §112, as the Examiner considers that there does not appear to be support for the lower logical address portion not having lock bits. Applicant has amended the claims to clarify that Claim 7 requires that there be a variable location (Claim 5) for storing the lock bits and that portions of the memory that are associated with lower logical addresses which do not contain the lock bits be erased before the topmost portion of the memory having a relatively higher logical address than the lower logical portion be erased. The topmost portion, i.e., the last page in the

associated section, is the one that contains the lock bits and, when that is erased, the lock bits will be erased. This is described with reference to Fig. 11, beginning at page 22, line 22. It is set forth that the variable location is where the lock bits are stored and they are typically in the upper portion of the memory in the reserve space (1102). At page 23, beginning at line 5, it is set forth that the user space lock byte is erased by erasing one logical block of memory at a time beginning at the lower end thereof until the user lock byte is erased at the upper end thereof. As such, Applicant believes that this portion of the specification clearly supports the operation as set forth in Claim 7, it being noted that the portions that are discussed as being erased that do not contain lock bits are the pages below the variable location and its associated page of memory space. Therefore, Applicant respectfully requests the withdrawal of the 35 U.S.C. §112 rejection with respect to Claim 7.

Claims 1-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hotley* and *Zimmer et al.* (*Zimmer*). This rejection is respectfully traversed with respect to the amended claims.

The *Hotley* reference has been described in previous Responses. However, a more detailed description that illustrates the distinctions may be useful in this Response. The *Hotley* reference in general is directed toward the concept of protecting blocks of memory on a block-by-block basis. Each memory location has a plurality of bits associated therewith, this typically being the address portion of the memory for output of data therefrom or storage of data therein. For example, if a memory location were eight bits wide, this would be an 8-bit memory location. To provide additional storage space for a given block, an additional bit of memory is provided for each memory location as a lock bit, such that each memory location in a block has one bit of the lock bits for that block. However, it is noted that this lock bit is not in the addressable memory space when reading data or writing data, as the particular column in which that particular lock bit is disposed is inhibited from being accessed after it is written to in a separate Write operation. Each block has associated with it a "key" that is utilized to determine if access to that block is allowed. Once the block access is initiated, it is necessary to sequentially read out all of the lock bits in that particular lock bit location. In essence, this constitutes a particular register that must be accessed and the contents thereof compared with a key word to determine if access is allowed. If this comparison is a true comparison, then access is allowed and, if it is false, access is

inhibited. Therefore, there is not provided a memory wherein each of the plurality of lock bits is stored in a separate logical portion of the memory space to determine access therefor. In *Hotley*, the lock bits are not contained within one of the separate portions of the memory space relating to more than the associated block; rather, each portion or block has a key word associated therewith that is disposed within that particular block and only associated with that block. Therefore, upon attempting to access a particular block, the lock register must first be examined to determine if this is permissible. Further, any erasure of the lock bits is inhibited, such that this must be a separate lock portion of the memory.

Compared to Applicant's present inventive concept, as defined by the amended claims, each logical portion is associated with a single lock bit, wherein all of the lock bits are stored in one of the memory portions of the memory space associated with at least one of the lock bits. Therefore, all the lock bits will be stored in a single logical portion of the memory space such that they can be operated on by the memory access operation. In *Hotley*, it can be seen that, once written, the lock bits are effectively protected from any memory access operation to data stored in the memory. By providing lock bits that are stored within the memory space of one of the logical sections in Applicant's device, all that is required is to access that memory location and then determine if access to other blocks is permissible for Read or Write operations. Of course, this presents a problem when erasing the memory in that some care must be taken not to erase the logical portion with the lock bits contained therein, but one of the memory portions can be erased without erasing the lock bit, as that lock bit is not stored in that position. Since that logical portion has associated therewith it a lock bit that defines access thereto, if that lock bit were set to allow erasure of that block to erase lock bits, it would destroy the integrity of the system with respect to the remaining data if that data were left intact. Therefore, *Hotley* would teach against storing the lock bits within one of the logical memory portions protected by a lock bit that defines whether a memory operation can be performed thereon.

The Examiner has added the *Zimmer* reference to disclose the use of separate lock bits, one for a Read lock and one for a Write lock. However, it is noted that a separate register is provided in *Zimmer* such that this separate register is not a part of the memory. Therefore, the lock bits can be loaded separately in this memory location during a boot operation to protect a boot block. Thus, there is no

provision to provide lock bits in the memory that, once stored, will prevent access to the memory wherein the portion that is locked contains the lock bits. As such, *Zimmer* does not cure the deficiencies noted hereinabove with respect to *Hotley*. Therefore, Applicant respectfully requests the withdrawal of the 35 U.S.C. §102(a) rejection with respect to Claims 1-7 in view of the combination of *Hotley* and *Zimmer*.

Claims 1-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hotley* in view of *Sharma et al.* (*Sharma*). This rejection is respectfully traversed.

The Examiner has utilized the *Sharma* reference to teach the use of a Read lock bit which would block access to the memory block from a predetermined access type, wherein the access lock type is a Read operation.

The *Sharma* device is associated with a cache. There is provided a status line that has a field that indicates whether a Read operation is locked. This is described beginning at Col. 6, line 45. This constitutes a variable that indicates that an I/O device has requested a corresponding cache line and the cache line has not yet been returned to the requesting I/O device. This is a distinctly different operation than associated with Applicant's present inventive concept, in that there is no protection of the particular memory but, rather, merely an inhibit operation to prevent contention between operations such that one device accessing the memory is not interrupted by another device attempting to access the memory. Thus, there is no disclosure of any operation wherein any memory has disposed therein lock bits, with each bit associated with a separate portion of the memory wherein the lock bits are stored in one of those portions of the memory. In fact, this particular status line is typically outside of the memory proper and is a separate memory that is read to determine what operations can or cannot be performed on a particular memory. Thus, Applicant believes that the combination of *Hotley* and *Sharma* does not anticipate or obviate Applicant's present inventive concept, as defined by the amended claims. Therefore, Applicant respectfully requests withdrawal of the 35 U.S.C. §103(a) rejection with respect to the combination of *Sharma* and *Hotley*.

Claims 1-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hotley* in combination with *Wolrich et al.* (*Wolrich*). This rejection is respectfully traversed.

The Examiner has utilized the *Wolrich* reference as disclosing in Fig. 3 thereof a Read lock bit that would lock access to the memory block from a predetermined access type. The *Wolrich* reference is a device that utilizes a content addressable memory (CAM) for the use of look-ups of Read blocks. This is a separate device that has a comparator associated therewith to provide a very fast operation, this type of memory typically being an associative memory. Therefore, there is no disclosure set forth therein for the use of lock bits, one bit associated with each portion of the memory to be locked and which lock bits are stored in at least one section of the memory. Therefore, Applicant believes that neither *Wolrich* and *Hotley*, taken singularly or in combination, obviate or anticipate Applicant's present inventive concept, as defined by amended Claims 1-7. Therefore, Applicant respectfully requests the withdrawal of the 35 U.S.C. §103(a) rejection with respect the combination of *Hotley* and *Wolrich*.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/CYGL-24,692 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
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